Claims

1-20 (canceled)

21. (New) A system , comprising:

a random access memory device;

a first signal line coupled to the random access memory device, the first signal line to carry a first signal;

a second signal line coupled to the random access memory device, the second signal line to carry a second signal; and

a memory controller coupled to the first signal line and the second signal line, wherein the memory controller includes a delay locked loop to generate the first signal, wherein the first signal is used to transmit data to the random access memory device, the delay locked loop to receive the second signal such that the second signal is used to sample read data provided by the memory device.

22. (New) The system as recited in claim 21, wherein the memory controller includes a driver such that the first signal is used to transmit data to the memory device by way of the driver.

23. (New) The system as recited in 21, wherein the memory controller includes a sampler to sample the read data using the second signal.

24. (New) The system as recited in claim 21, further comprising:

a first delay element coupled in a feedback path of the delay-locked loop to change a phase difference between the second signal and a reference clock signal by a first time period.

25. (New) The system as recited in claim 24, further comprising:

a second delay element outside the feedback path of the delay-locked loop

to receive the second signal, and

to delay the first signal relative to the second signal by the first time period.

26. (New) The system of claim 21, further including a clock generator to generate the second signal, wherein the second signal propagates from the clock generator to the memory controller.

27. (New) The system of claim 26, wherein the second signal is terminated after being received by the memory controller.

28. (New) The system of claim 21, wherein the first signal is a clock signal and the second signal is a clock signal.

29. (New) The system as recited in claim 21, wherein the delay-locked loop further includes a phase detector to identify phase differences between the second signal and the reference clock signal.

30. (New) The system as recited in claim 29, wherein the phase detector is a zero phase detector.

31. (New) The system as recited in claim 29, wherein the phase detector is an integration sampler to integrate the first signal with respect to the reference clock signal.

32. (New) The system as recited in claim 21, wherein the delay-locked loop further includes a 180 degree phase shift circuit to adjust a phase of the second signal.

33. (New) The system as recited in claim 32, wherein the 180 degree phase shift is accomplished by switching over the first signal line and the second signal line.

34. (New) The system as recited in claim 21, wherein first data of the read data is sampled on a rising edge of the second signal and second data of the read data is sampled on a falling edge of the second signal.

35. (New) The system as recited in claim 21, wherein the delay lock loop generates a receive clock using the second signal, wherein the receive clock is used to sample read data by way of the second signal.

36. (New) The system of claim 35, wherein the delay locked loop generates the receive clock such that a phase of the receive clock is aligned with a phase of the second signal.

37. (New) A method of operation in a memory controller comprising:

generating a first signal using a single delay-locked loop wherein the first signal is used to time data transmission;

changing a phase difference between the first signal and a reference signal by a first time period using a second delay element outside the feedback path of the delay-locked loop circuit; and

receiving a second signal to be delayed relative to the first signal by the first time period using a first delay element in a feedback path of the delay-locked loop, wherein the second signal is used to time data reception.

38. (New) The method as recited in claim 37, further comprising transmitting data by way of a driver.

39. (New) The method as recited in 37, further comprising sampling the read data using the second signal.

40. (New) The method as recited in claim 37, further comprising changing a phase difference between the second signal and a reference clock signal by a first time period.

41. (New) The method as recited in claim 40, further comprising delaying the first signal relative to the second signal by the first time period.

42. (New) The method of claim 37, further comprising generating the second signal from a clock generator and propagating the second signal to a memory controller.

43. (New) The method of claim 42, further comprising terminating the second signal after the second signal is received by the memory controller.

44. (New) The method of claim 37, wherein the first signal is a clock signal and the second signal is a clock signal.

45. (New) The method as recited in claim 37, further comprising identifying phase differences between the second signal and the reference clock signal.

46. (New) The method as recited in claim 45, further comprising detecting a zero phase difference.

47. (New) The method as recited in claim 45, further comprising integrating the first signal with respect to the reference clock signal.

48. (New) The method as recited in claim 37, further comprising adjusting a phase of the second signal by 180 degrees.

49. (New) The method as recited in claim 48, further comprising switching over the first signal line and the second signal linc to effect the 180 degree phase shift.

50. (New) The method as recited in claim 37, wherein first data of the read data is sampled on a rising edge of the second signal and second data of the read data is sampled on a falling edge of the second signal.

51. (New) The method as recited in claim 37, further comprising generating a receive clock using the second signal, wherein the receive clock is used to sample read data by way of the second signal.

52. (New) The method of claim 51, further comprising generating the receive clock such that a phase of the receive clock is aligned with a phase of the second signal.

53. (New) A system, comprising:

an electronic data store;

a controller for the electronic data store, including:

a delay-locked loop to receive a second signal, wherein the delay-locked loop includes:

a first delay element coupled in a feedback path of the delay-locked loop, wherein the first delay element changes a phase difference between the second signal and a reference clock signal by a first time period, and

a second delay element outside the feedback path to receive the second signal and output a first signal that is delayed relative to the second signal by the first time period; and

a phase detector to determine phase differences between the second signal and the reference clock signal.

54. (New) The system as recited in claim 53, wherein the phase detector comprises a zero phase detector.

55. (New) The system as recited in claim 53, wherein the delay-locked loop further includes a 180 degrees phase shifter.

56. (New) The system as recited in claim 53, wherein the first and second signals provide timing for address multiplexing operations of the electronic data store.

57. (New) The system as recited in claim 53, further comprising an integration sampler to integrate the first signal with respect to the reference clock signal.

58. (New) A system, comprising:

means for electronic storage of data; and

means for controlling the electronic storage of data, including:

means for generating a first signal and a second signal, the means for generating including:

a first means for delaying data transfer of the second signal to be used for changing a phase difference between the second signal and a reference clock signal by a first time period, and

a second means for delaying data transfer of the first signal to be used for receiving the second signal and outputting the first signal that is delayed relative to the second signal by the first time period.